Claims:

1. (Original) A pipeline memory device comprising:

a plurality of memory cells that store data;

a data transfer path on which the data is transferred;

a data fetching control circuit that is configured to generate:

a first pipeline control signal, in response to a first clock signal for generating the first pipeline control signal: and

a second pipeline control signal, in response to both a second clock signal for generating the second pipeline control signal and the first pipeline control signal;

a first pipeline stage that latches the data on the data transfer path in response to the first pipeline control signal;

a second pipeline stage that latches the data latched by the first pipeline stage in response to the second pipeline control signal; and

a third pipeline stage that outputs the data latched by the second pipeline stage to a data output pad in response to a data output clock signal.

2. (Original) The pipeline memory device of claim 1, wherein the data fetching control circuit comprises:

a first edge trigger delay circuit that receives the first clock signal for generating the first pipeline control signal and generates the first pipeline control signal; and

a multiplexer that receives the second clock signal for generating the second pipeline control signal and the first pipeline control signal, and generates the second pipeline control signal.

3. (Currently Amended) The pipeline memory device of claim 2, wherein the first ~~and second edge trigger delay circuits compromise~~ edge trigger delay circuit compromises an even number of inverters in a chain.

4. (Original) The pipeline memory device of claim 1, wherein the data fetching control circuit comprises:

a first edge trigger delay circuit that receives the first clock signal for generating the first pipeline control signal and generates the first pipeline control signal;

a second edge trigger delay circuit that receives the second clock signal for generating the second pipeline control signal;

a first inverter that inverts the first pipeline control signal;

a NAND gate that receives the output of the first inverter and the second edge trigger delay circuit; and

a second inverter that inverts the output of the NAND gate to output the second pipeline control signal.

5. (Original) The pipeline memory device of claim 4, wherein the first and second edge trigger delay circuits compromise an even number of inverters in a chain.

6. (Original) A data fetching method for a pipeline memory device, comprising:

transferring data stored in memory cells along a transfer path;

generating a first pipeline control signal in response to a first clock signal for generating a first pipeline control signal;

generating a second pipeline control signal in response to a second clock signal for generating a second pipeline control signal and the first pipeline control signal;

latching the data to a first pipeline stage on the transfer path in response to the first pipeline control signal;

latching the data to a second pipeline stage on the transfer path in response to the second pipeline control signal; and

outputting the data from the second pipeline stage to a data output pad in response to a data output clock signal.

7. (Original) The method of claim 5, wherein a point of activation of the second pipeline control signal is determined depending on a point of activation of the first pipeline control signal.

8. (Original) The method of claim 5, wherein the second pipeline control signal is activated when the first pipeline control signal is inactive.

9. (Original) An apparatus comprising:

at least one memory cell;

a first pipeline stage coupled to the output of the at least one memory cell, wherein the first pipeline stage is driven by a first control signal; and

a second pipeline stage coupled to the output of the first pipeline stage, wherein the second pipeline stage is driven by the first control signal and a second control signal.

10. (Original) The apparatus of claim 9, wherein the first control signal and the second control signal are driven by a clock signal.

11. (Original) The apparatus of claim 10, wherein the clock signal is an internal clock signal.

12. (Original) The apparatus of claim 10, wherein:

the first control signal is delayed from the clock signal by a first delay; and

the second control signal is delayed from the clock signal by a second delay.

13. (Original) The apparatus of claim 12, wherein the first delay is larger than the second delay.

14. (Original) The apparatus of claim 9, wherein the first control signal and the second control signal are never in an active state at the same time.

15. (Currently Amended) The apparatus of claim 9, wherein the second pipeline stage is driven by the first control signal, and the second control signal ~~utilizing~~ utilizes a multiplexer.

16. (Currently Amended) The apparatus of claim 9, wherein the second pipeline stage is driven by the first control signal, and the second control signal ~~utilizing~~ utilizes a NAND gate.